Wide Optical Spectrum Laser Power Monitor IC

ISL58327

The ISL58327 photo sensor IC has a wide optical spectral sensitivity from 400nm to 1000nm. It is good for multiple light source applications, such as laser based projectors. The ISL58327 has two banks of three sets of gain registers. For a Pico-Projector application, the two banks of gain registers can be used to monitor the bias level and peak level of each wavelength. Bank switching is done by applying a TTL compatible logic signal to the HL pin. The three sets of gain registers can be used to adjust optical-to-electrical conversion gain for each RED, GREEN, and BLUE laser or any wavelength in a spectral range for application. The ISL58327 is a single die device that has a photo detector of 0.7mm diameter in the center of the die. The photo current signal is amplified through the TIA, fine gain amplifier, and the output drivers to convert from current to voltage. The output of ISL58327 can be configured to be either differential or single-ended. Gain changing according to each wavelength is done through the I^2C serial interface. Registers can be updated in real time while the device is in operation.

The ISL58327 operates from a single +5V supply. It is available in a space-saving 9-ball glass top BGA package.

Features

- High Sensitivity from 400nm to 1000nm with Patented Technology for Improved Blue Photo Response
- Differential Voltage Output or Single-Ended Output
- Internal Output Reference or External Output Reference
- Serial Interface for Gain Calibration
- Fast Settling Time < 20ns
- Wide Signal Bandwidth > 80MHz
- Wide Signal Gain Dynamic Range > 20dB
- Low Power Consumption
- Low Output Offset < 50mV
- Small 9-Ball Optical Chip Scale Package (OCSP) (3mmx3mm)
- I^2C Serial Interface

Applications

- Optical Power Monitoring
- Laser Based Pico-Projectors or Projection TV
- Laser Auto Power Control for Laser Based Application
- White Balance for LED Based LCoS and DLP Pico Projectors

Related Literature

- See TB478 “PCB Assembly Guidelines for Shell-Op 3D Package”

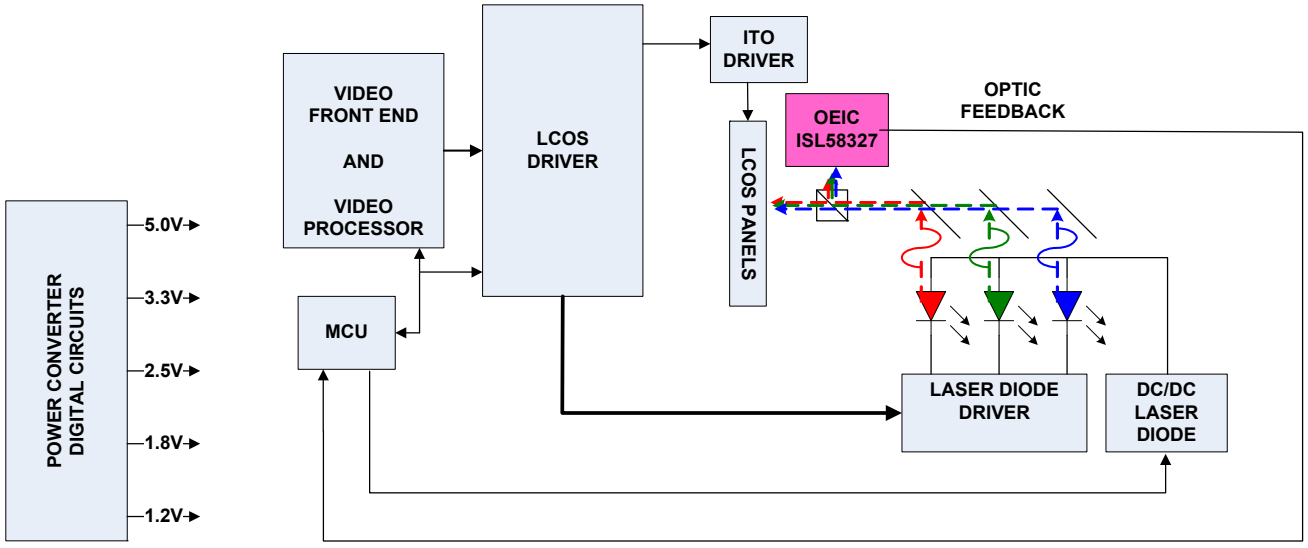
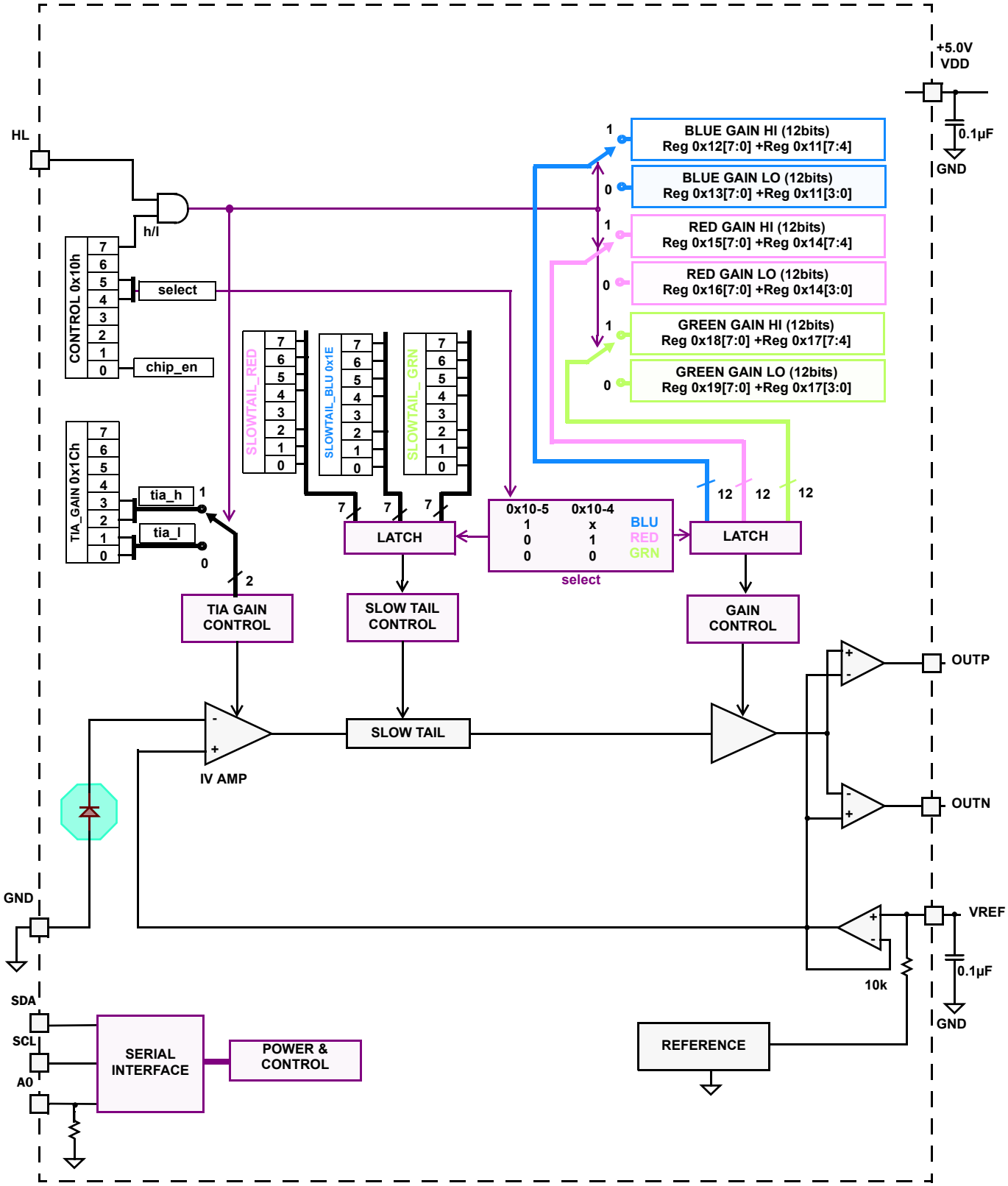


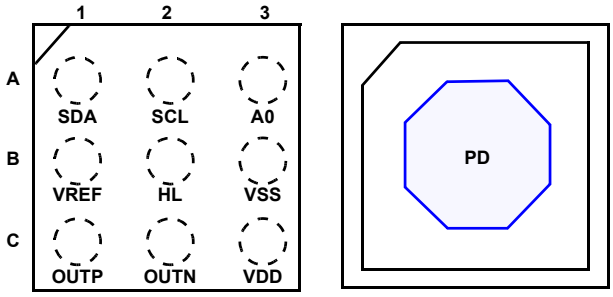
FIGURE 1. APPLICATION BLOCK DIAGRAM

Block Diagram



Pin Configuration

ISL58327
(9 BALL OCSP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
A1	SDA	Digital I/O	I^2C interface data, bi-directional
B1	VREF	Analog Input	Reference voltage input
C1	OUTP	Analog Output	Positive swing analog output
A2	SCL	Digital Input	Serial interface clock
B2	HL	Digital Input	HIGH/LOW gain mode selection, H = High gain, L = Low Gain. Use in conjunction with Reg 0x10 bit 7. * For hard switching, Reg 0x10 bit 7 must be set to 1. * For soft switching, this pin must be High.
C2	OUTN	Analog Output	Negative swing analog output
A3	A0	Digital Input	I^2C address A0; internally pulled down.
B3	VSS	Power	GND
C3	VDD	Power	+5.0V supply
-	PD	Optical input	Photo diode

Ordering Information

PART NUMBER (Notes 1, 2, 3, 4)	PACKAGE Tape & Reel (Pb-free)	PKG. DWG. #
ISL58327CIZ-T7	9 Ball OCSP	S3x3.9
ISL58327CIZ-T7A	9 Ball OCSP	S3x3.9

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Please refer to TB478 for solder profile.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL58327. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage (+5.0V to GND) 6.0V
Maximum CMOS Input/Output 5V
Maximum Output Voltage . . . . . V_{SS} - 0.3 to V_{DD} + 0.3
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). 2kV
Machine Model (Per EIAJ ED-4701 Method C-111) 200V
Latch Up (Tested per JESD-78; Class II; Level A) 100mA

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} (°C/W)
9 Ld OCSP 125
Storage Temperature Range . . . . . -25°C to +125°C
Pb-Free Reflow Profile . . . . . 250°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
T_A	Ambient Temperature		0	25	85	°C
T_{DIE}	Die Temperature		0	50	125	°C

DC Electrical Specifications V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_{VDD1}	Supply Current	No incident light, in normal mode		20	25	mA
I_{VDD1}	Supply Current	No incident light, in SLEEP mode			600	µA
V_{OFS}	Output Offset, Referenced to VREF	No incident light	-50	9	+50	mV
V_{REF_i}	Common Mode Output Voltage	Internal VREF generator	1.75		2.35	V
V_{IL}	CMOS Input LOW	SDA, SCL, and HL pins	V_{GND}		0.8	V
V_{IH}	CMOS Input HIGH	SDA, SCL and HL pins	3.3		5.0	V

AC Electrical Specifications V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OUTMAX}	Differential Mode Output Voltage (OUTP) – (OUTN)	Linear output		2.95		V_{P-P}
Bandwidth	Bandwidth OUTP, OUTN (not differential)	-3dB RBW = 30kHz		85		MHz

Sensitivity V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$Gain_{00}$	TIA Lowest Gain (445nm)	0dB fine gain adjustment, 7FFh Differential output	350	450	550	mV/µA
$Gain_{01}$	TIA 2nd Lowest Gain (445nm)	0dB fine gain adjustment, 7FFh Differential output	700	890	1100	mV/µA
$Gain_{10}$	TIA 2nd Highest Gain (445nm)	0dB fine gain adjustment, 7FFh Differential output	1400	1790	2170	mV/µA
$Gain_{11}$	TIA Highest Gain (445nm)	0dB fine gain adjustment, 7FFh Differential output	3700	4850	6020	mV/µA
$Gain_{Fine\_MAX}$	Maximum Fine Gain	for both HIGH Gain and LOW Gain channels Compared to 0dB fine gain setting, 7FFh		19		dB
$Gain_{Fine\_MIN}$	Minimum Fine Gain	for both HIGH Gain and LOW Gain channels Compared to 0dB fine gain setting, 7FFh		-5.5		dB
Current to Optical conversion: Optical sensitivity is not tested in production. Gain parameters were obtained using input test currents. The following factors are used to convert current to optical power.						
$I2O_{450nm}$	Current to Optical conversion (450 nm)	Bench data; measured on typical devices		0.27		µA/µW
$I2O_{530nm}$	Current to Optical conversion (530 nm)	Bench data; measured on typical devices		0.26		µA/µW
$I2O_{640nm}$	Current to Optical conversion (640 nm)	Bench data; measured on typical devices		0.38		µA/µW

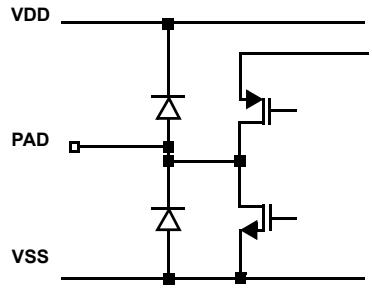
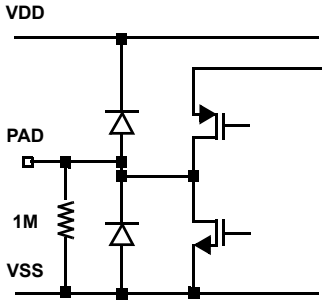
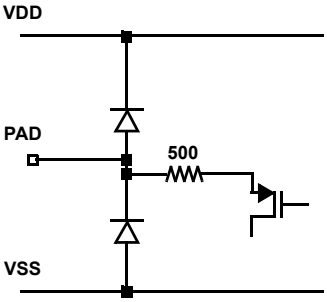
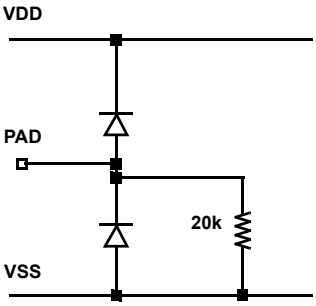
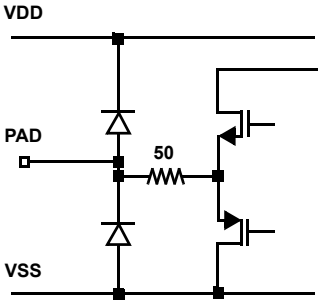
Serial Interface AC Performance V_{DD} = 5.0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
C_i	Input Capacitance				10	pF
f_{SCL}	SCL Clock Frequency				400	kHz
$INPUT_{LEAKGE}$	Input Leakage SCL and SDA pin		-20		20	µA

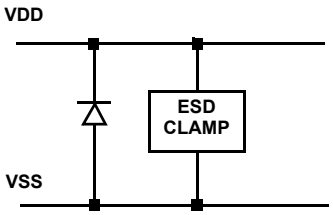
NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

I/O Pins Equivalent Circuits

PINS	TYPE	EQUIVALENT CIRCUIT
SDA SCL	Digital I/O Digital Input	
A0	Digital Input	
H/L	Digital Input	
VREF	Analog Input	
OUTP OUTN	Analog Output	

I/O Pins Equivalent Circuits (Continued)

PINS	TYPE	EQUIVALENT CIRCUIT
VDD	Power	

Application Information

Input Optical Power

The ISL58327 has a photo detector in an octagon shape (shown in PD pattern) with 700µm diameter. It is sensitive from 400nm to 1000nm for light power monitoring application, which is a perfect choice for Light Automatic Power control. This wide range of sensitivity also allows the ISL58327 to be used for white balance control in systems such as LED based LCoS or DLP pico projectors.

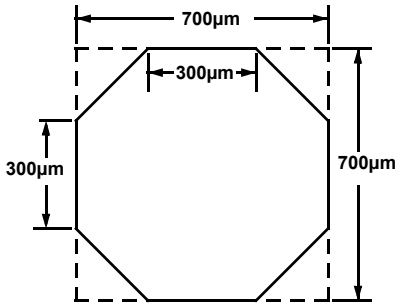
Current generated by the photo detector, is amplified by a trans-impedance amplifier (TIA). The TIA has four feedback resistors; the user can choose which feedback resistor is used for HIGH or LOW gain applications by the setting in tia_gain register. Once an appropriate resistor is selected for the required TIA gain, the optical signal is then amplified by the TIA, which feeds into the fine gain stage. HIGH gain channel and LOW gain channel TIA gains can be individually set through the TIA register. The HIGH gain and LOW gain channels have the same gain adjustment range (20dB) and can be individually controlled.

In applications, if light power is modulated between 2 power levels, the user can choose between HIGH gain channel for low power level and LOW gain channel for high power. It can provide the best resolution when power is low yet the amplifier circuit is not saturated when the power is high. If users do not need to monitor two power levels, there is no need to switch between the HIGH gain channel and LOW gain channel. The selection of HIGH gain or LOW gain signal path can be done with fast hardware switching or by setting the register bit “h/l”. When changing HIGH Gain or LOW Gain signal paths by hardware switching, “h/l” bit needs to be “1”; when changing it with the register (soft switching), the HL pin needs to be driven by digital HIGH because HL and “h/l” are AND’ed for TIA gain control. Regardless of the channel gain settings, the dynamic range of TIA is determined by the photo detector sensitivity with respect to wavelength. For example, in a 445nm application when TIA = 01b gain is selected, the maximum input optical power is limited to 2mW for blue light laser, but this limitation is reduced to 1.45mW with a 638nm laser. This is because the photo detector has a higher optical-to-electrical conversion efficiency at longer wavelengths. Higher than the maximum input limitation, the TIA or whole device will still be working but it may yield a distorted output and a long falling time, while the circuits recover from saturation.

TABLE 1. MAXIMUM INPUT POWER vs TIA RESISTOR

TIA_Gain (tia_h/tia_l)	(445nm) mW	(638nm) mW	(532nm) mW
00b	5.0	3.65	5.30
01b	2.5	1.82	2.65
10b	1.25	0.91	1.33
11b	0.44	0.32	0.47

Detector Pattern



Gain Control

The ISL58327 channel gain is set through a 12-bit DAC, separated into 2 registers. Each wavelength has two 12-bit gain registers; one for HIGH gain applications and the other for LOW gain applications. The selection of HIGH gain or LOW Gain is done by fast hardware switching through the HL pin or “h/l” register bit. All gain registers of HIGH Gain and LOW Gain channels are capable of update at anytime through the serial interface. The 12-bit gain registers provide a total of 25dB of adjustment range; +16dB to -5.5dB reference to fine gain setting 7FFh. All settings will be reset to default at power-on. The user needs to load all gain settings after the ISL58327 is powered up. Overall differential output signal gain can be estimated by using Equations 1 through 3:

Blue Laser Diode(445nm)

$$\text{Gain}\ (\text{mV}/\mu\text{W}) = \frac{1.88 \times \text{TIA}}{256 + \text{Code}} \quad \text{(EQ. 1)}$$

Red Laser Diode (638nm)

$$\text{Gain}\ (\text{mV}/\mu\text{W}) = \frac{2.57 \times \text{TIA}}{256 + \text{Code}} \quad \text{(EQ. 2)}$$

Green Laser Diode(530nm)

$$\text{Gain}\ (\text{mV}/\mu\text{W}) = \frac{1.76 \times \text{TIA}}{256 + \text{Code}} \quad \text{(EQ. 3)}$$

Where: Code is 12 bits fine gain code in decimal (0 ~ 4095) and TIA is the factor shown in Table 2.

TABLE 2. TIA FACTOR IN EQUATIONS

tia_h, tia_l SETTINGS	TIA FACTOR IN EQUATION
00b	500
01b	1000
10b	2000
11b	5400

Output Configuration

The ISL58327 has two differential outputs: OUTP is a positive and OUTN is a negative swing output. OUTP and OUTN outputs are referenced to VREF. VREF can be externally supplied or from the internally generated 2.1V. With respect to the input optical signal, OUTP swings up from the reference voltage and OUTN swings down from the reference voltage. Both OUTP and OUTN have the same linear output dynamic range up to 1.4V swing

from the reference voltage. When using an external reference voltage, the user needs to adjust the gain registers to set proper channel gain to prevent output saturation. To use ISL58327 as a single-ended output, the user can take either OUTP or OUTN signal and load the unused output with the equivalent resistor and capacitor load to keep both outputs with the same loading condition. However, it is acceptable to leave the unused output floating. It is not recommended to use VREF as a reference source to drive other devices. To obtain the best signal quality at the input of the AFE, it is recommended to keep OUTP and OUTN traces in parallel and to keep them with same length, width, and routing. If output signals from ISL58327 need to travel through a flex cable to the AFE, matching with the impedance of flex cable is necessary. The best value should be determined according to the actual application.

Slow Tail Compensation

Photons at longer wavelengths will penetrate deeper into the photo detector structure than photons at shorter wavelengths. It takes more time for electron-hole pairs to become photo current and results in longer response of pulse outputs, called slow tail. Longer wavelength light such as 638nm or IR has more visible slow tail effect than blue light. To minimize the slow tail effect, ISL58327 has incorporated Intersil's proprietary slow tail compensation technology. There are three registers for slow tail compensation adjustment for each wavelength (638nm, 532nm, and 445nm). Slow tail compensation function is not limited to the specific wavelength listed previously; it is in conjunction with the selected fine gain registers. The user can disable slow tail compensation by setting Bit 7 (MSB) of the register to "0". This function can also be used to improve the quality of the pulse output waveforms due to impedance mismatch from the OEIC outputs to the flex. One example is to improve Tr/Tf or to minimize overshoot.

Layout Consideration

When using differential output, layout the OUTP and OUTN traces next to each other. The ground trace should be placed to another side of the OUTP and OUTN traces. When using single-ended, the reference trace needs to be laid out next to the output signal trace. The ground trace should be laid out on the other side of the output. For best results, a dual layer flex with signal on one side and the ground plane on another side is a must.

Reference Voltage

The ISL58327 has a built-in reference voltage generator to generate 2.1V reference voltage for all circuit blocks. Output is biased at the internal reference voltage automatically when the VREF pin is left floating. When a DC voltage is applied to the VREF pin, OUTP and OUTN will be biased at the external reference voltage. External reference should be within the range of 1.5V to 2.5V. Outside of this range may yield distorted outputs. When using external reference voltage, good decoupling is very important to prevent noise coupling into VREF. A 0.1µF ceramic capacitor placed as close to the VREF pin as possible is recommended to decouple VREF to ground.

Power Supply Decoupling

Due to the current being switched rapidly at OUTP and OUTN, it is important to ensure that the power supply is well decoupled to ground. During output switching, the V_{DD} undergoes severe current transients, thus every effort should be made to decouple the V_{DD} as close to the package as possible.

Without proper power supply decoupling, the result could be poor rise/fall times, overshoot, and poor settling response.

Sensitivity Curves

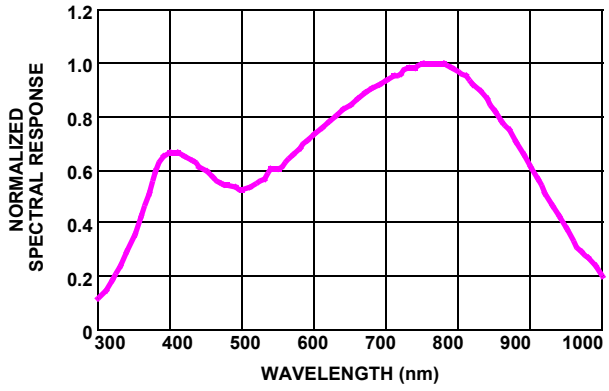


FIGURE 2. NORMALIZED SPECTRAL RESPONSE vs WAVELENGTH

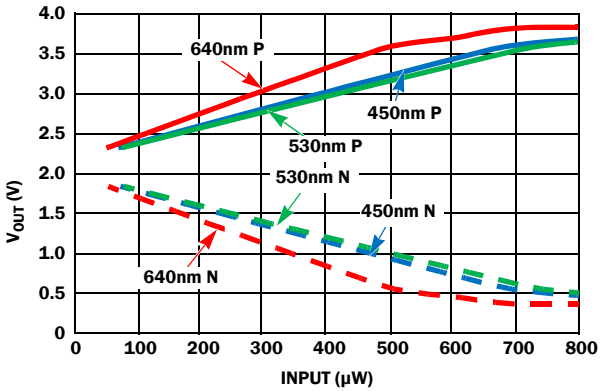


FIGURE 3. INTENSITY vs OUTPUT (RED LED 620nm; GREEN LED 532nm; BLUE LED 460nm)

Register Map

ADDR	NAME	b7	b6	b5	b4	b3	b2	b1	b0	DEFAULT	ACCESS
00h	ID0	DEVICE ID								27h	R
01h	ID1	DEVICE OPTION				DEVICE VERSION				E0h	R
02h		reserved									
03h		reserved for multi-chip protocol									
04h		reserved for multi-chip protocol									
05h		reserved for multi-chip protocol									
06h		reserved for multi-chip protocol									
07h		reserved for multi-chip protocol									
08h		reserved for multi-chip protocol									
09h		reserved for multi-chip protocol									
0Ah		reserved for multi-chip protocol									
0Bh		reserved for multi-chip protocol									
0Ch		reserved for multi-chip protocol									
0Dh		reserved for multi-chip protocol									
0Eh		reserved for multi-chip protocol									
0Fh		reserved for multi-chip protocol									
10h	CONTROL	h/l	deglitch_b	blue	red/green	test_en	x	x	chip_en	06h	RW
11h	B _GAIN0	blue_h[3: 0]				blue_l[3:0]				FFh	RW
12h	B_H_GAIN	blue_h[11:4]								7Fh	RW
13h	B_L_GAIN	blue_l[11:4]								7Fh	RW
14h	R_GAIN0	red_h[3:0]				red_l[3:0]				FFh	RW
15h	R_H_GAIN	red_h[11:4]								7Fh	RW
16h	R_L_GAIN	red_l[11:4]								7Fh	RW
17h	GREEN_GAIN0	green_h[3:0]				green_l[3:0]				FFh	RW
18h	GREEN_H_GAIN	green_h[11:4]								7Fh	RW
19h	GREEN_L_GAIN	green_l[11:4]								7Fh	RW
1Ah	ST_RED	st_en_red	st_time_red[2:0]			x	st_mag_red[2:0]			00h	RW
1Bh	ST_GREEN	st_en_green	st_time_green[2:0]			x	st_mag_green[2:0]			00h	RW
1Ch	TIA_GAIN	x	x	x	x	tia_h[1:0]		tia_l[1:0]		00h	RW
1Dh		reserved									
1Eh	ST_BLUE	st_en_blue	st_time_blue[2:0]			x	st_mag_blue[2:0]			00h	RW

Note: All gain registers in this table can be used for any wavelength in spectral range from 390nm to 1000nm, not limited to wavelengths specified.

Register Description

TABLE 3. ID0 (addr = 00h)

REGISTER	DESCRIPTION
ID0	Device ID, read only, code = 27h

TABLE 4. ID1 (addr = 01h)

REGISTER	DESCRIPTION
DEVICE OPTION	Device option code, read only, code = E0h
DEVICE VERSION	Device version code, read only, code = 0h

TABLE 5. CONTROL (addr = 10h)

REGISTER	DESCRIPTION
h/l	HIGH gain or LOW Gain channels selection. Used in conjunction with HL pin. 1b: HIGH Gain channel 0b: LOW Gain channel Default: 0b
deglitch_b	1b: Disable serial interface deglitch function 0b: Enable serial interface deglitch function Default: 0b
blue	1b: Device works in blue mode (regardless of red/green bit setting) 0b: Device works in either RED or GREEN mode, depends on red/green register bit setting Default: 0b
red/green	0b: GREEN 1b: RED Default: 0b (GREEN mode)
test_en	To enable a chip test function (for Intersil internal use only) 1b: Enable test function 0b: Disable test function Default: 0b
chip_en	To enable or disable ISL58327. When disabled all outputs are in Hi-Z 1b: enable 0b: disable (SLEEP mode)

TABLE 6. B_GAIN0 (addr = 11h)

REGISTER	DESCRIPTION
blue_h[3: 0]	Lower 4 bits of blue light HIGH Gain channel fine gain control
blue_l[3: 0]	Lower 4 bits of blue light LOW Gain channel fine gain control

TABLE 7. B_H_GAIN (addr = 12h)

REGISTER	DESCRIPTION
blue_h[11:4]	High 8 bits of blue light HIGH Gain channel fine gain control

TABLE 8. B_L_GAIN (addr = 13h)

REGISTER	DESCRIPTION
blue_l[11:4]	High 8 bits of blue light LOW Gain channel fine gain control

TABLE 9. RED_GAIN0 (addr = 14h)

REGISTER	DESCRIPTION
red_h[3: 0]	Lower 4 bits of red light HIGH Gain channel fine gain control
red_l[3: 0]	Lower 4 bits of red light LOW Gain channel fine gain control

TABLE 10. RED_H_GAIN (addr = 15h)

REGISTER	DESCRIPTION
red_h[11:4]	High 8 bits of red light HIGH Gain channel fine gain control

TABLE 11. RED_L_GAIN (addr = 16h)

REGISTER	DESCRIPTION
red_l[11:4]	High 8 bits of red light LOW Gain channel fine gain control

TABLE 12. GREEN_GAIN0 (addr = 17h)

REGISTER	DESCRIPTION
green_h[3:0]	Lower 4 bits of green light HIGH Gain channel fine gain control
green_l[3:0]	Lower 4 bits of green light LOW Gain channel fine gain control

TABLE 13. GREEN_H_GAIN (addr = 18h)

REGISTER	DESCRIPTION
green_h[11:4]	High 8 bits of green light HIGH Gain channel fine gain control

TABLE 14. GREEN_L_GAIN (addr = 19h)

REGISTER	DESCRIPTION
green_l[11:4]	High 8 bits of green light LOW Gain channel fine gain control

TABLE 15. ST_RED (addr = 1Ah)

REGISTER	DESCRIPTION
st_en_red	Red light slow tail compensation control 1b: enable 0b: disable (when disable, st_time_red and st_mag_red are reset to 000b)
st_time_red	Red light slow tail compensation time constant control
st_mag_red	Red light slow tail compensation magnitude control

TABLE 16. ST_GREEN (addr = 1Bh)

REGISTER	DESCRIPTION
st_en_green	Green light slow tail compensation control 1b: enable 0b: disable (when disabled, st_time_green and st_mag_green are reset to 000b)
st_time_green	Green light slow tail compensation time constant control
st_mag_green	Green light slow tail compensation magnitude control

TABLE 17. TIA_GAIN (addr = 1Ch)

REGISTER	DESCRIPTION
tia_l[1:0]	TIA gain selection in LOW Gain channel application 00b: Lowest gain 01b: 2nd lowest gain 10b: 2nd highest gain 11b: Highest gain
tia_h[1:0]	TIA gain selection in HIGH Gain channel application 00b: Lowest gain 01b: 2nd lowest gain 10b: 2nd highest gain 11b: Highest gain

TABLE 18. ST_BLUE (addr = 1Eh)

REGISTER	DESCRIPTION
st_en_blue	Blue light slow tail compensation control 1b: enable 0b: disable (when disable, st_time_blue and st_mag_blue are reset to 000b)
st_time_blue[2:0]	Blue light slow tail compensation time constant control
st_mag_blue[2:0]	Blue light slow tail compensation magnitude control

Serial Interface Protocol

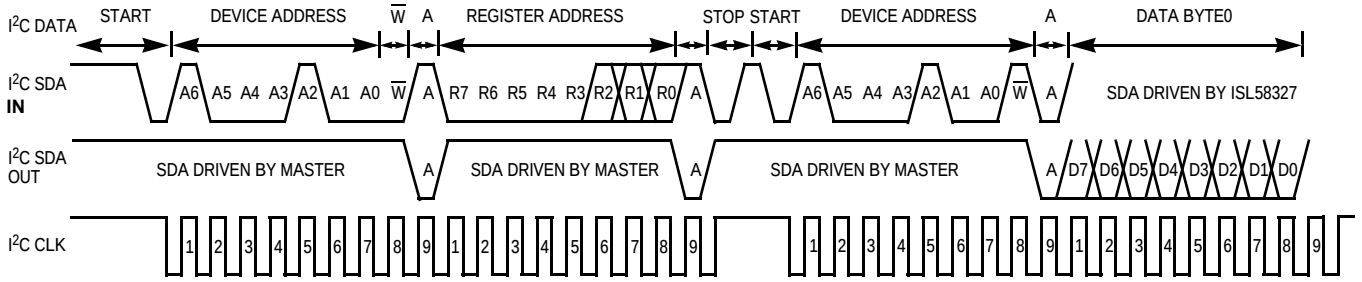


FIGURE 4. I²C READ TIMING DIAGRAM SAMPLE

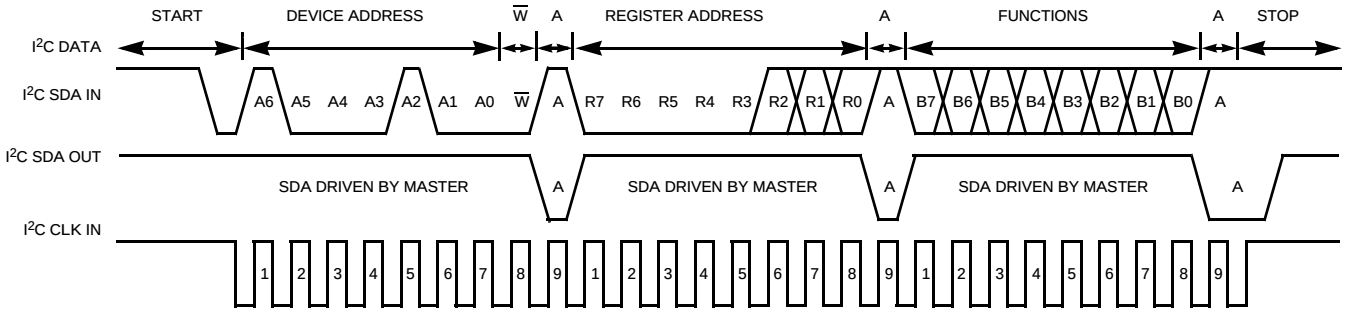


FIGURE 5. I²C WRITE TIMING DIAGRAM SAMPLE

I²C Interface

The device address of the I²C bus of the ISL58327 is a 7 bits fixed address 0011_10(A0)xb, where (A0) can be hard wired. Note that (A0) is internally pulled down. When 001110(A0)x with x as R or W is sent after the Start condition, this device compares the first seven bits of this byte to its address and matches. Since SCL and SDA lines of the I²C bus are either open collector or open drain, 2 pull-up resistors (Rp)on bus for SCL and SDA are necessary. To minimize crosstalk and to minimize spikes, a serial termination resister (Rs) close to the SCL and SDA lines are important for each device on the I²C bus. The value of Rp and Rs is determined according to the maximum sink current of the device, supply voltage, bus capacitance, and the number of devices on the bus. Even though the maximum bus capacitance of the fast mode specified in the I²C bus is 400pF, it is always recommended to reduce bus capacitance to get better signal quality.

Figure 4 shows a sample one-byte read. Figure 5 shows a sample one-byte write. For more information about the I²C standard, please consult the Philips™ I²C specification documents.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 29, 2013	FN6577.2	Changed Product information verbiage to About Intersil verbiage.
February 21, 2012	FN6577.1	Added ISL58327CIZ-T7A to “Ordering Information” on page 3.
August 30, 2011	FN6577.0	Initial release.

About Intersil

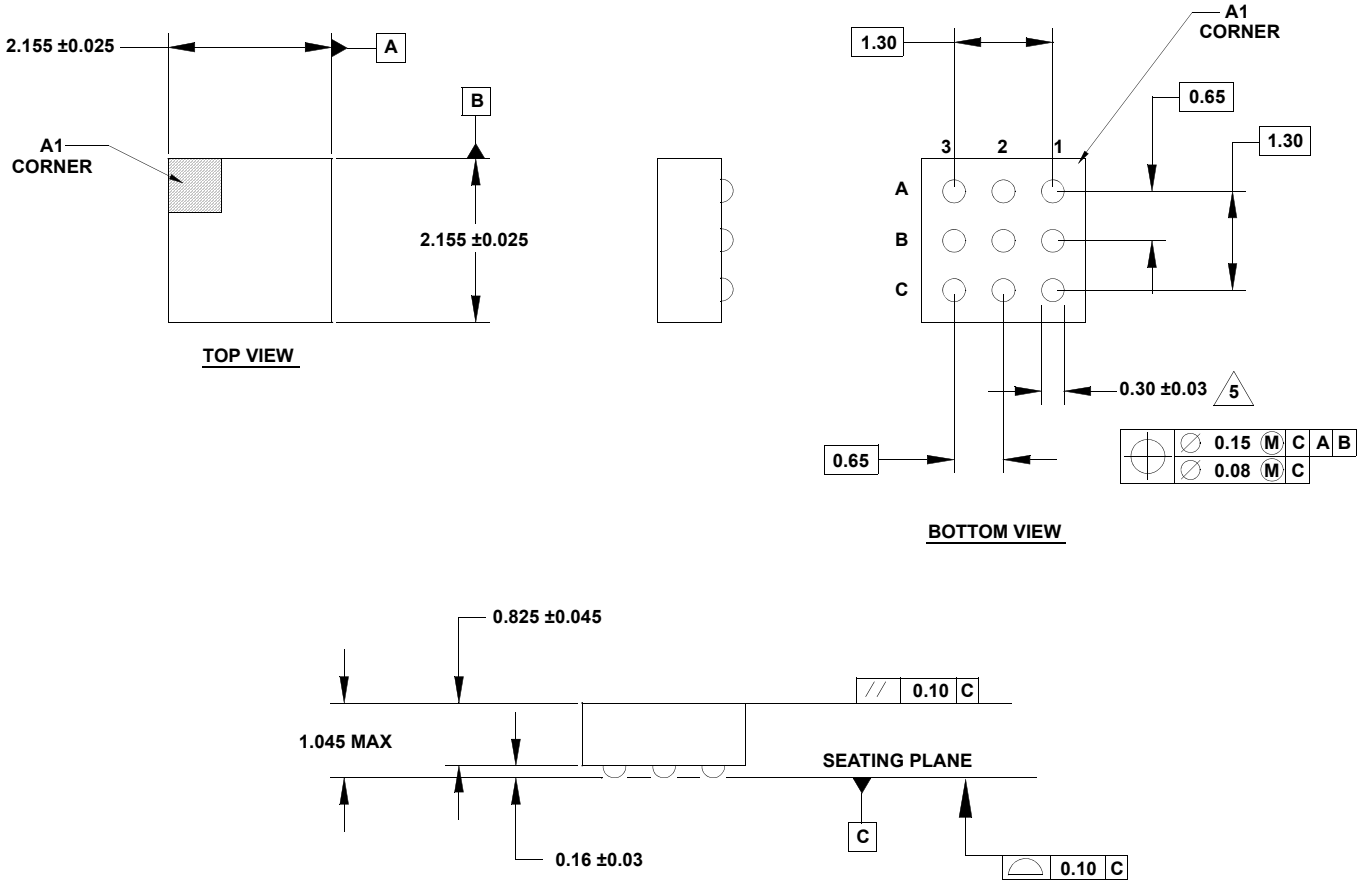
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

S3x3.9

3X3 ARRAY 9 BUMP OPTICAL CHIP SCALE PACKAGE (OCSP)
Rev 7, 10/10



NOTES:

1. **Dimensions are in millimeters.**
   Dimensions in ( ) for Reference only.
2. **Dimensioning and tolerancing conform to ASME Y 14.5M-1994**
3. **Primary datum C and seating plane are defined by the spherical crowns of the contact balls.**
4. **Pin "A1" is marked on the top and bottom side adjacent to the A1 ball.**
5. **Dimension is measured at the maximum ball diameter.**