Turbo Encoder

User's Guide

November 2008
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Introduction

This document contains technical information about the Lattice Turbo Encoder IP core.

Turbo coding is an advanced error correction technique widely used in the communications industry. The Turbo Encoder IP Core offered by Lattice is compliant with three different standards: 3GPP, 3GPP2 and CCSDS.

The Turbo Encoder core comes with the following documentation and files:

- User's Guide
- Lattice evaluation gate level netlist
- Evaluation model for simulation
- Core instantiation template
- Testbench and testbench coding template

Core Specification

Features

- Fully compatible with Third Generation Partnership Project (3GPP) standard:
  - 3GPP TS 25.212 Version 4.2.0
- Fully compatible with Third Generation Partnership Project 2 (3GPP2) standard:
  - 3GPP2 C.S0002-A
- Fully compatible with Consultative Committee for Space Data Systems standard:
  - CCSDS 101.0-B-5
- Configurable input block sizes
- User defined number of states
- User parameterized forward and backward polynomials
- Programmable puncturing support
- Fixed processing delay of 12 cycles for CCSDS, 10 cycles for 3GPP, and 9 cycles for 3GPP2

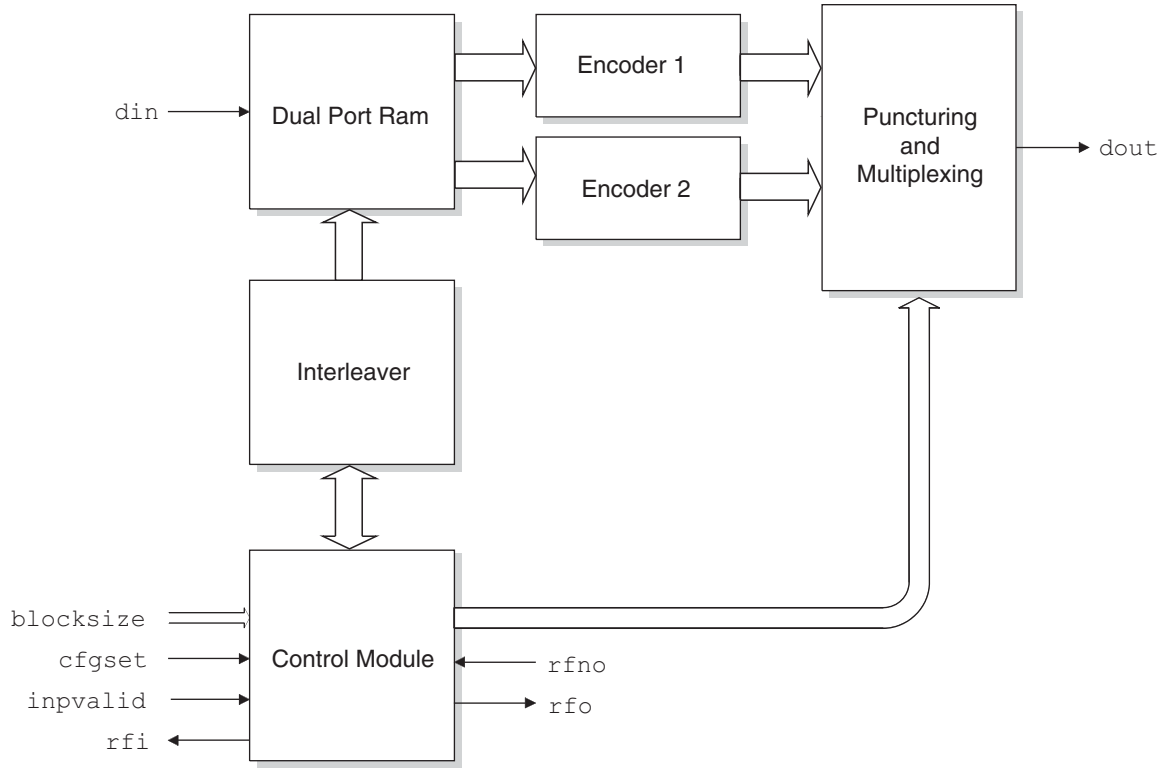
General Description

Turbo encoders and decoders are key elements in today's communication systems to achieve the best possible data reception with least possible errors. Lattice's Turbo Encoder IP Core is compliant with three different standards: 3GPP, 3GPP2, and CCSDS. The 3GPP and 3GPP2 standards are widely used in WCDMA and MC-CDMA applications while CCSDS is most commonly used in telemetry and space communications. Each one of these encoders is a separate entity as the interleaver and control logic for each encoder is completely different.

Lattice's Turbo Encoder core is created in conjunction with the Turbo Decoder core to provide users with a state of the art error correction technique. For more information on Lattice products, refer to the Lattice website at www.latticesemi.com.

Block Diagram

Figure 1. Turbo Encoder Internal Block Diagram



Signal Description

Figure 2. Turbo Encoder I/O Diagram

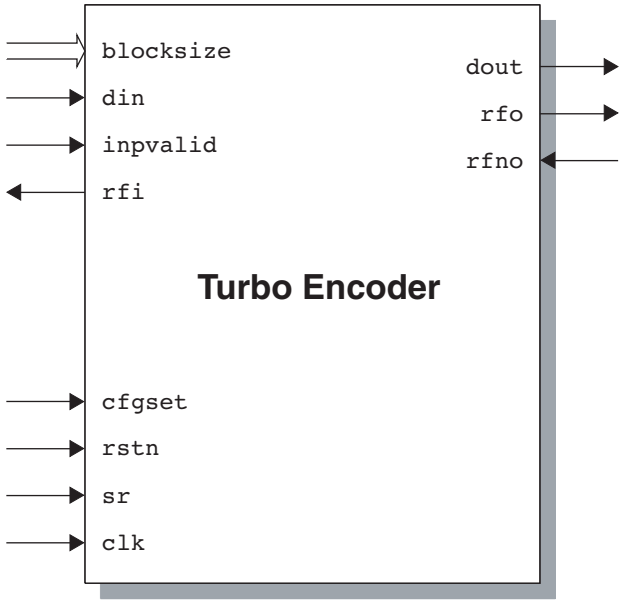


Table 1. Turbo Encoder Signal Definitions

Port Name	I/O Type	Width	Signal Description
clk	Input	1	System Clock
rstn	Input	1	Active Low Asynchronous Reset
sr	Input	1	Synchronous Reset
din	Input	1	Data Input
dout	Output	1	Data Output
cfgset	Input	1	Interleaver initialization. blocksize on input pins is accepted when this signal is asserted.
inpvalid	Input	1	Enables the encoder to read the data at din when asserted.
blocksize	Input	13-15	Block size up to 20730 bits can be set depending on the configuration. Block size ranges: 3GPP: 40-5114 3GPP2: 378-20730 CCSDS: 1784, 3568, 7136, 8920
rfi	Output	1	This signal is asserted when the encoder is ready to read from din. It is de-asserted one clock cycle before the last input data is read in.
rfno	Input	1	Asserted to indicate successful reading of encoded data from dout.
rfo	Output	1	When asserted encoded data is ready and available at dout.

User Configurable Parameters

User configurable parameters for each standard are shown below in Table 2. These parameters are configured using IPexpress™, included with Lattice's ispLEVER® design tools.

Table 2. User Configurable Parameters

Parameter	3GPP	3GPP2	CCSDS
Encoder Type	THREE_GPP	THREE_GPP2	CCSDS
Number of States	8	8	16
Forward Polynomial for Encoder 1	N/A	Default: 1101	Default: 11011
Reverse Polynomial for Encoder 1	N/A	Default: 1011	Default: 10011
Forward Polynomial for Encoder 2	N/A	Default: 1101	Default: 11011
Reverse Polynomial for Encoder 2	N/A	Default: 1011	Default: 10011
Code Rate	1/3	Range: 1/2, 1/3, 1/4 Default: 1/3	Range: 1/2, 1/3, 1/4, 1/6 Default: 1/3
Maximum Block Size	Default: 5114	Range: 4096-20730 Default: 20730	Range: 1784, 3568, 7136, 8920 Default: 8920
Fixed Block Size	N/A	N/A	Values: Yes or No Default: No

Functional Description

The Turbo Encoder functions as a slave device with respect to the input source, which applies the inputs to the encoder, as well as the output source, which takes the encoded data from the encoder. Data is fed through two recursive systematic convolutional (RSC) encoders. Each RSC encoder contains the same structure but operates on two different versions of data. The first encoder operates on an original copy of data, whereas the second encoder operates on an "interleaved" version of data. Interleaving is the method in which bits are rearranged according to a predefined algorithm.

The Lattice Turbo Encoder IP Core consists of four different modules: Control Module, Dual Port RAM, Encoder Module and Interleaver Module.

Control Module

The control module takes care of the handshake and control signals necessary for communication between the various blocks and I/O pins. The block size is determined by the user and input into the control module. Signal `cfgset` enables the data on `blocksize` to be latched into the encoder. In order for a change in `blocksize` to be recognized, `cfgset` must be asserted.

Control signals `rfi` and `rfo` are generated to indicate when the Turbo Encoder is ready to accept new data and ready to output encoded data. `rfi` is an active high signal and is activated only when the encoder is ready to accept data. Once `rfi` goes low, `rfo` is asserted after a fixed processing delay to output encoded data. After data on `din` is valid, signal `inpvalid` can be asserted by the user to allow the encoder to read data. `inpvalid` should be asserted only when `rfi` is high except for the last data to be input. In the same manner signal `rfno` should be asserted by the user to read encoded data only when `rfo` is high.

Signal `sr` can be used to reinitialize the Turbo Encoder in the middle of a block processing. This can be done at any point of time during the operation of the encoder. If `sr` is asserted it should be followed by an initialization of `cfgset` to specify the `blocksize` and start the encoding process all over again. Input signal `rstn` is an asynchronous reset. This clears all the flip-flops in the design.

Dual Port RAM and Interleaver Module

The dual port RAM module stores the incoming data block. Each memory size is equal to the data block size. After the encoder receives all the data in a block, the interleaving process begins.

The interleaver module is required to randomize the bit positions in the block. The interleaver is a mapping between input and output bit positions and involves a predefined algorithm that changes the position of the bits. This algorithm is implemented in the interleaver module. Interleaving begins once a full block of data is received and stored into the dual port RAM. All computation needed for interleaving is completed before any data comes in. A copy of the incoming data goes directly to the first encoder while an interleaved copy goes to the second encoder.

The Lattice Turbo Encoder IP Core has a fixed processing delay which is smaller than most competing solutions. Once the data is received, the encoder is ready (after the fixed processing delay) to output the encoded data. The processing delay is not dependent on the block size selected.

Encoder Module

The encoder module consists of two recursive systematic convolutional (RSC) encoders. At the output of the two encoders is a multiplexer, which selects the output from different paths depending upon the output rate specified. If non-standard forward and reverse feedback connections are required, they may be implemented in the encoder by user-defined forward and reverse polynomials.

Code Rate (Puncturing and Termination)

Code rate is defined as the ratio of number of data bits to the total number of bits in the output of the encoder. In turbo codes, puncturing can increase the code rate. A puncturing pattern defines the position of parity bits to be omitted from the encoded stream. At the decoder, knowledge of this pattern enables de-puncturing. The Turbo Encoder IP Core supports programmable puncturing.

In turbo codes Convolutional Code Termination is used so data can be treated in a block-by-block fashion. After the data block has been encoded special termination bits are inserted in the encoder to initialize its state to an all zero state. During termination, output bits are appended to the data stream, and thus the "actual" code rate is slightly less than the nominal rate. Termination bits in the output stream are not punctured in order to enable the decoder state initialization.

Figures 3, 4 and 5 illustrate the timing specifications of the Turbo Encoder IP Core.

Figure 3 shows the Turbo Encoder signals after an asynchronous reset and a new block size input. The signal `cfgset` is asserted high when the block size information is placed on `blocksize` port. The encoder asserts `rfi` to indicate that it is ready to accept new data. Then the user places data on `din` port and also pulls `inpvalid` high to indicate the presence of a valid data to the encoder. After the encoder receives all but one data in a block, it de-asserts `rfi` signal. The user can only place one more new data after the encoder de-asserts `rfi`. After the `rfi` goes low, the encoder takes a fixed number of clock cycles (tagged as "processing delay" in the figure) before it can output the encoded data. The encoder asserts `rfo` to signify the availability of encoded data at the output. The first encoded data is then read out by the user. As the `rfno` remains high in the following cycles, the encoder continues to output successive data.

Figure 3. Turbo Encoder After Reset and First Data Block Input

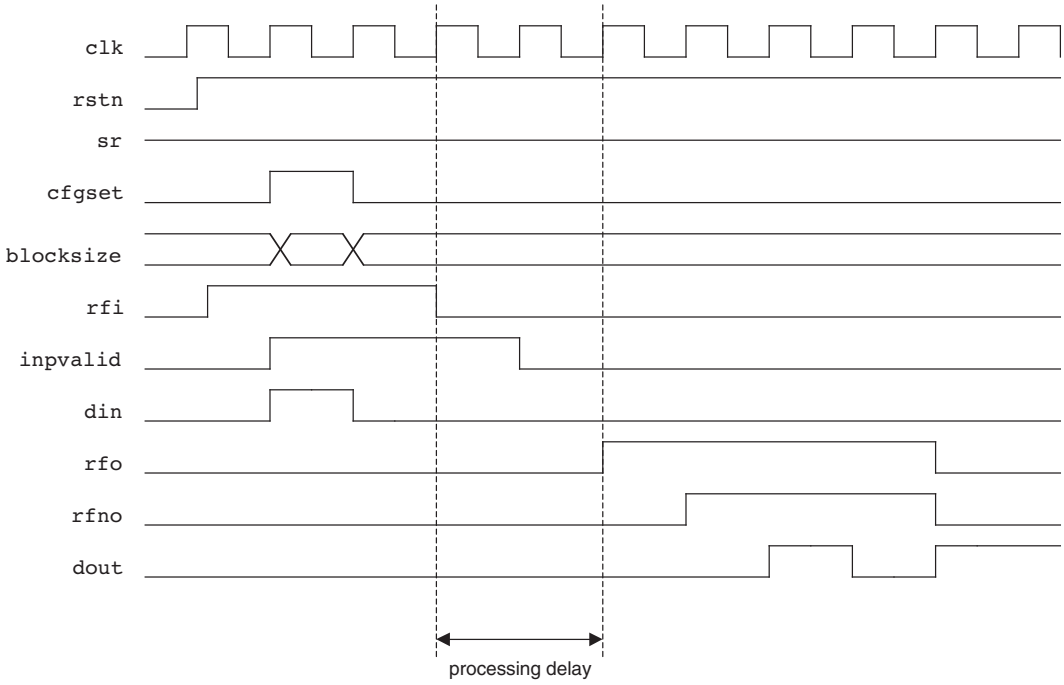


Figure 4 shows the handshaking signals during a discontinuous input and output data flow. In the figure the signal `inpvalid` is de-asserted to signify the data on `din` is not valid. Similarly, the signal `rfno` is de-asserted to indicate the user is not ready to read the next data. The encoder suspends giving out new data due to this.

Figure 4. Handshake Signals for Discontinuous Data Flow

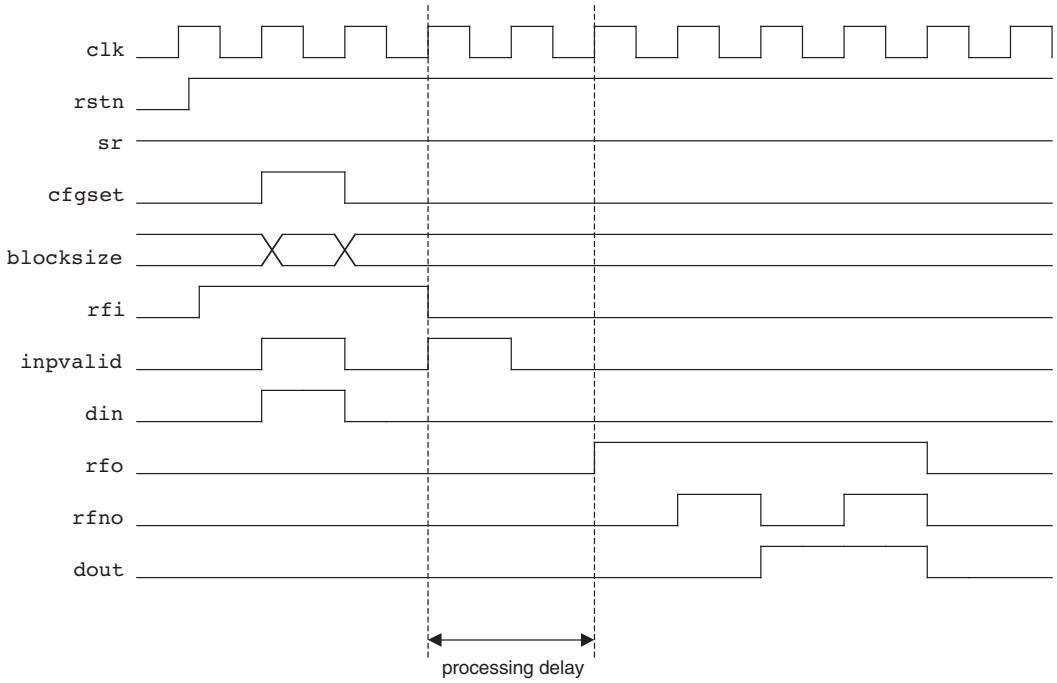
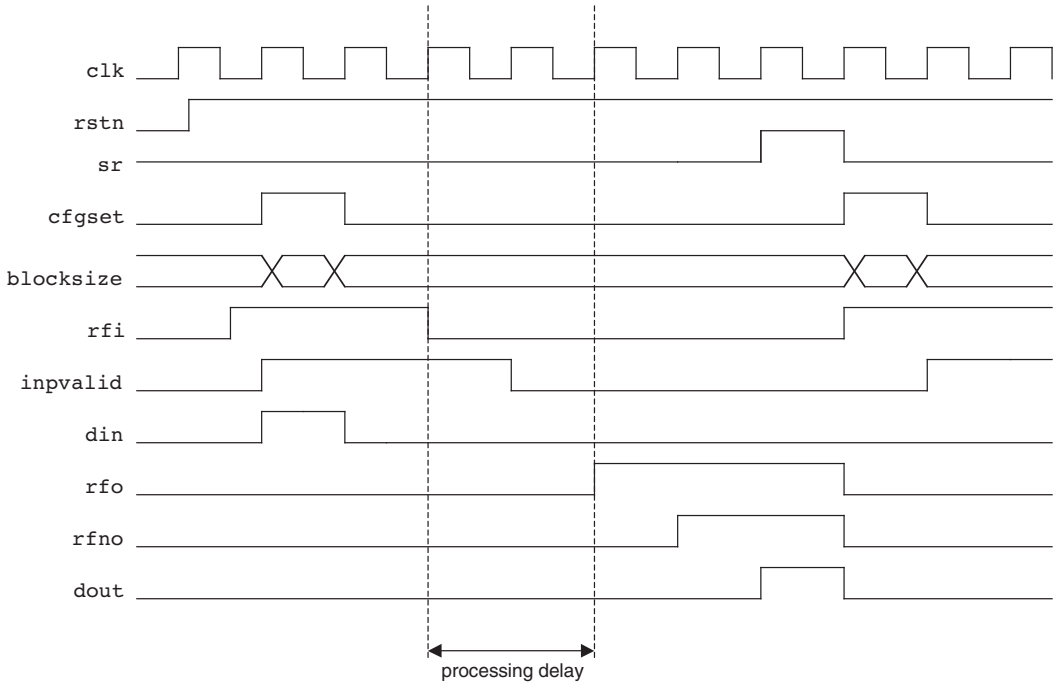


Figure 5 depicts the case when signal `sr` is used. Signal `sr` is used to reinitialize the Turbo Encoder and can be done at any point of time during the operation of the encoder. When `sr` is asserted, signal `cfgset` is then asserted to specify the `blocksize` and start the encoding process all over again.

Figure 5. Turbo Encoder with Synchronous Reset



IPexpress User-Configurable Core

The Turbo Encoder core is an IPexpress User-Configurable IP core, which allows designers to configure the IP and generate netlists as well as simulation files for use in designs. The IPexpress flow also supports a hardware evaluation capability, making it possible to create versions of the IP core that operate in hardware for a limited period of time without requiring the purchase of an IP license. To download a full evaluation version of this IP core, please go to the Lattice IP Server tab in the ispLEVER IPexpress GUI window. All ispLeverCORE™ IP cores available for download are visible on this tab.

Reference Information

- ispLEVER Software Online Help Manual

The Lattice Turbo Encoder IP Core is compliant with three standards: 3GPP, 3GPP2 and CCSDS. More information about each standard can be referenced at the following locations.

- The 3rd Generation Partnership Project (www.3gpp.org) provides specifications to 3GPP TS 25.212 v4.2.0 (2001-09) standards.
- The 3rd Generation Partnership Project 2 (www.3gpp2.org) provides specifications to 3GPP2 C.S0002-A standards.
- The Consultative Committee for Space Data Systems (www.ccsds.org) provides specifications to CCSDS 101.0-B-5 standards.

Technical Support Assistance

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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
November 2006	04.1	Added support for LatticeECP2, LatticeXP and LatticeSC FPGA families.
December 2006	04.2	Updated appendices. Added support for LatticeECP2M FPGA family.
June 2007	04.3	Updated appendices. Added support for LatticeXP2 FPGA family.
November 2008	04.4	Updated appendices.

Appendix for Series 4 ORCA® FPGAs and FPSCs

Table 3. Performance and Utilization[1]

Parameter File	Mode	Parameters	ORCA4 PFUs	LUTs	Registers	PIO	EBR	f_{MAX}
turbo_enco_o4_1_001.lpc	3GPP	See Table 1	328	1774	694	23	1	62 MHz
turbo_enco_o4_1_002.lpc	3GPP2	See Table 1	107	555	324	25	3	70 MHz
turbo_enco_o4_1_003.lpc	CCSDS	See Table 1	97	250	393	24	2	66 MHz

1. Performance and utilization characteristics are generated targeting an OR4E02-2BA352 in ispLEVER® 3.0 software.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting ORCA Series 4 devices is TURBO-ENCO-O4-N1. Table 3 lists the netlists that are available in Evaluation Package, which can be downloaded from the Lattice web site at www.latticesemi.com.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Table 4. IP Core Configurations

Configuration	3GPP (config 1)	3GPP2 (config 2)	CCSDS (config 3)
Blkwidth	13	15	14
StandBlkSizeFix	NA	NA	0
EncoderType	3GPP	3GPP2	CCSDS
Rate	1/3	1/3	1/3
FWDNUM	1	1	1
STATENUM	8	8	16
MAXBLKSIZE	5114	20730	8920
E1_FWD_Poly1	NA	1101	11011
E1_FWD_Poly2	NA	NA	NA
E1_FWD_Poly3	NA	NA	NA
E2_FWD_Poly1	NA	1101	11011
E2_FWD_Poly2	NA	NA	NA
E2_FWD_Poly3	NA	NA	NA
E1_REV_Poly1	NA	1101	10011
E2_REV_Poly1	NA	1101	10011
FWD_Poly1	1101	NA	NA
FWD_Poly2	NA	NA	NA
FEW_Poly3	NA	NA	NA
REV_Poly1	1011	NA	NA
USE_GSR	1	1	1

Table 4 lists some configurations available for the Turbo Encoder IP core. These configurations are IPexpress User-Configurable for LatticeECP/EC, LatticeECP2™, LatticeECP2M™, LatticeXP™, and LatticeSC™ devices. Using IPexpress, any configuration can be generated for these device families.

Appendix for ispXPGA® FPGAs

Table 5. Performance and Resource Utilization[1]

Parameter File	Mode	Parameters	ispXPGA PFUs	LUTs	Registers	PIO	EBR	f_{MAX}
turbo_enco_xp_1_001.lpc	3GPP	See Table 4	469	1222	550	23	6	61MHz
turbo_enco_xp_1_002.lpc	3GPP2	See Table 4	268	780	354	25	6	64MHz
turbo_enco_xp_1_003.lpc	CCSDS	See Table 4	208	432	436	24	4	93MHz

1. Performance and utilization characteristics are generated targeting an LFX500B-04F516C in Lattice ispLEVER 3.x software. The evaluation version of this IP core only works on this specific device density, package, and speed grade

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting ispXPGA devices is TURBO-ENCO-XP-N1. Table 5 lists the netlists that are available in Evaluation Package, which can be downloaded from the Lattice web site at www.latticesemi.com.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Appendix for LatticeECP™ and LatticeEC™ FPGAs

Table 6. Performance and Resource Utilization[1]

Parameter File	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	f_{MAX} (MHz)
3GPP	692	1363	452	23	4	99
3GPP2	352	678	320	25	4	123
CCSDS	263	492	384	24	2	177

1. Performance and utilization characteristics are generated using LFECP20E-5F672C, with Lattice's ispLEVER 7.1 SP1 software. When using this IP core in a different density, speed, or grade within the LatticeECP/EC family, performance and utilization may vary.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting LatticeECP devices is TURBO-ENCO-E2-U3. Table 4 lists the parameter settings that are available for the Turbo Encoder.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Appendix for LatticeECP2™ FPGAs

Table 7. Performance and Resource Utilization[1]

Parameter File	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	f_{MAX} (MHz)
3GPP	691	1365	450	23	4	135
3GPP2	356	686	322	25	2	202
CCSDS	275	516	378	24	1	256

1. Performance and utilization characteristics are generated using LFE2-20E-7F672C, with Lattice's ispLEVER 7.1 SP1 software. When using this IP core in a different density, speed, or grade within the LatticeECP2 family, performance and utilization may vary.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting LatticeECP2 devices is TURBO-ENCO-P2-U3. Table 4 lists the parameter settings that are available for the Turbo Encoder.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Appendix for LatticeECP2M™ FPGAs

Table 8. Performance and Resource Utilization[1]

Parameter File	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	f_{MAX} (MHz)
3GPP	691	1365	450	23	4	143
3GPP2	356	686	322	25	2	204
CCSDS	275	516	378	24	1	246

1. Performance and utilization characteristics are generated using LFE2M-35E-7F484C, with Lattice's ispLEVER 7.1 SP1 software. When using this IP core in a different density, speed, or grade within the LatticeECP2M family, performance and utilization may vary.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting LatticeECP2M devices is TURBO-ENCO-PM-U3. Table 4 lists the parameter settings that are available for the Turbo Encoder.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Appendix for LatticeXP™ FPGAs

Table 9. Performance and Resource Utilization[1]

Parameter File	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	f_{MAX} (MHz)
3GPP	692	1363	452	23	4	94
3GPP2	352	678	320	25	2	123
CCSDS	263	492	384	24	1	177

1. Performance and utilization characteristics are generated using LFXP20E-5F484C, with Lattice's ispLEVER 7.1 SP1 software. When using this IP core in a different density, speed, or grade within the LatticeXP family, performance and utilization may vary.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting LatticeXP devices is TURBO-ENCO-XM-U3. Table 4 lists the parameter settings that are available for the Turbo Encoder.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Appendix for LatticeXP2™ FPGAs

Table 10. Performance and Resource Utilization[1]

Parameter File	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	f_{MAX} (MHz)
3GPP	691	1365	450	23	4	119
3GPP2	356	686	322	25	2	176
CCSDS	275	516	378	24	1	222

1. Performance and utilization characteristics are generated using LFXP2-17E-7F484C, with Lattice's ispLEVER 7.1 SP1 software. When using this IP core in a different density, speed, or grade within the LatticeXP family, performance and utilization may vary.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting LatticeXP2 devices is TURBO-ENCO-X2-U3. Table 4 lists the parameter settings that are available for the Turbo Encoder.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Appendix for LatticeSC™ FPGAs

Table 11. Performance and Resource Utilization[1]

Parameter File	SLICEs	LUTs	Registers	I/Os	sysMEM EBRs	f_{MAX} (MHz)
3GPP	691	1349	448	23	4	184
3GPP2	361	690	322	25	2	220
CCSDS	275	516	386	24	1	325

1. Performance and utilization characteristics are generated using LFSC3GA25E-7F900C, with Lattice's ispLEVER 7.1 SP1 software. When using this IP core in a different density, speed, or grade within the LatticeSC family, performance and utilization may vary.

Ordering Part Number

The Ordering Part Number (OPN) for all configurations of the Turbo Encoder core targeting LatticeSC devices is TURBO-ENCO-SC-U3. Table 4 lists the parameter settings that are available for the Turbo Encoder.

You can use the IPexpress software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.